

INGENIC®

T41

Hardware design guide

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Release history

Date	Revision	Change
Jun. 2022	1.0	First release
Sep.2022	1.1	1. Add VDDCORE&DDR voltage ripple description 2. Delete JTAG interface description
Oct.2022	1.2	1. DVP interface is changed to support only 10bit 2. The description of power supply and channel is added to SADC interface

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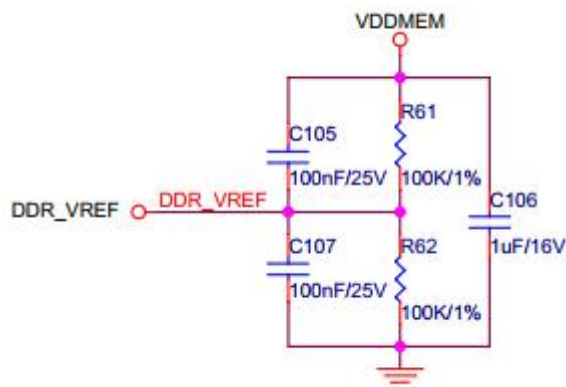
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1 Precautions for schematic design

DDR

- 1) DDR_ZQ: connect 240Ω 1% resistance to the ground.
- 2) RZQ: connect 240 Ω 1% resistance to the ground.
- 3) VREF divides the voltage, which is obtained from vddmem. The voltage dividing resistance is 1K~100K 1%, and the decoupling capacitance is 100nF.



Power Supply

1) The high frequency impedance of the power supply is related to the induction coefficient of the power supply. Multi stage capacitor filtering shall be added between DDRVDD, VDDMEM, VDDCORE and ground, such as 10uf+0.1uf+0.01uf, which can increase the filtering range of capacitance and reduce the high-frequency impedance on the power supply.

2) If a module is not required in the product, the magnetic beads of the power pin can be omitted, but the power supply cannot be omitted.

3) Power division of T41

Symbol	Description	Min	Typical	Max	Unit
VDDMEM	VDDMEM voltage for SSTL18(DDR2)	1.35	1.35	1.98	V
VDDMEM	VDDMEM voltage for SSTL18 (DDR3(L))	1.283	1.35/1.5	1.65	V
DDRVDD	DDR KGD power supplies voltage(DDR2)	1.62	1.8	1.98	V
DDRVDD	VDDMEM voltage for SSTL18 (DDR3(L))	1.283	1.35/1.5	1.65	V
DDRPLL_VCCA	DDR PLL Power supplies voltage	1.62	1.8	1.98	V
VDDIO2	GPIO power domain 2 supplies voltage	1.5	1.8/3.3	3.63	V
VDDIO1_1	GPIO power domain 1 supplies voltage	3.0	3.3	3.63	V

VDDIO1_2	GPIO power domain 1 supplies voltage	3.0	3.3	3.63	V
VDDIO18_1	GPIO power domain 0 supplies voltage	1.62	1.8	1.98	V
VDDIO18_1	GPIO power domain 0 supplies voltage	1.62	1.8	1.98	V
VDD	VDD core supplies voltage	0.72	0.8	0.88	V
PLL_AVDD	PLL analog voltage	1.62	1.8	1.98	V
VDD_RTC	Logic power supply for RTC	0.72	0.8	0.88	V
VDDIO_RTC	RTC IO analog voltage	1.62	1.8	3.63	V
EFUSE_AVDD	EFUSE program supplies voltage	1.62	1.8	1.98	V
SADC_AVDD	SAR-ADC analog voltage	1.62	1.8	1.98	V
CSI_VCC08	MIPI RX CORE analog voltage	0.72	0.8	0.88	V
CSI_VCC18	MIPI RX IO analog voltage	1.62	1.8	1.98	V
USB_AVD08	USB PHY VCCCORE analog voltage	0.72	0.8	0.88	V
USB_AVD18	USB PHY VCC18 analog voltage	1.62	1.8	1.98	V
USB_AVD33	USB PHY VCCA3P3 analog voltage	3.0	3.3	3.6	V
CODEC_AVDD	CODEC analog voltage	1.62	1.8	1.98	V

VDDCORE requires a power supply capacity of not less than 2A, the ripple noise on the chip is required to be controlled within 60mV; and VDDMEM/DDRVDV requires a power supply capacity of not less than 1A; USB_AVD33、USB_AVD18、USB_AVD08、DDRPLL_VCCA、PLL_AVDD、SADC_AVDD、CSI_VCC08、CSI_VCC18、CODEC_AVDD uses magnetic beads (1K Ω @100mhz) to isolate from other power supplies of the same level.

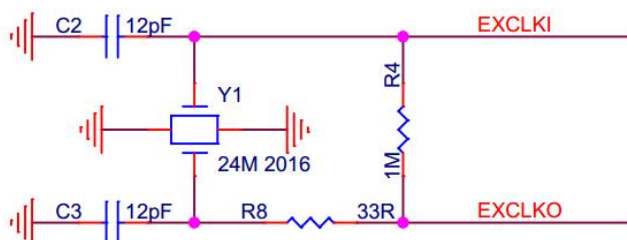
Boot mode of T41

BOOT_SEL1	BOOT_SEL0	Boot From
0	0	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C)
0	1	SFC boot @ CS4 (SFC boot @ SFC0&SFC1)
1	1	USB boot
1	0	UART boot @ CS2(Ymodem@115200/9600)

Support commonly used SFC boot and SD boot.

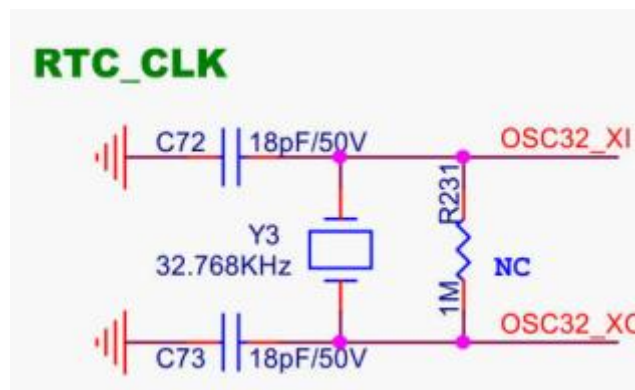
Main Clock

T41 requires an external 24MHz working clock with a maximum deviation of 30ppm. Typical circuits are as follows:



RTC Clock

T41 requires an external 32.768KHz working clock, and the external crystal has a great impact on the timing accuracy. It is necessary to use a suitable crystal in combination with crystal frequency offset, temperature and other factors. If the product requires very strict timing accuracy, it is recommended to build an external high-precision RTC circuit.



DVP interface

T41 supports 10bit DVP interface, which is distributed in PA groups PA00~PA17 of GPIO. Different sensors can be connected according to the following methods:

- 1) When the sensor is a 8 bit data interface, it needs to be connected to DVP0 to DVP7 from low to high.
- 2) When the sensor is a 10 bit data interface, it needs to be connected to DVP0 to DVP9 from low to high.

The DVP interface power domain of T41 is VDDIO18_2, only IO voltage of 1.8V is supported. DVP interface multiplexes BT656 input interface and BT1120 input interface at the same time (8bit serial mode). For specific GPIO multiplexing relationship, please refer to <<T41 IPC product GPIO recommended allocation table>>. It is worth noting that the IO drive capabilities of CMOS sensors from different manufacturers are different. During the design, pay attention to whether the DVP interface reserves resistance capacitance matching devices.

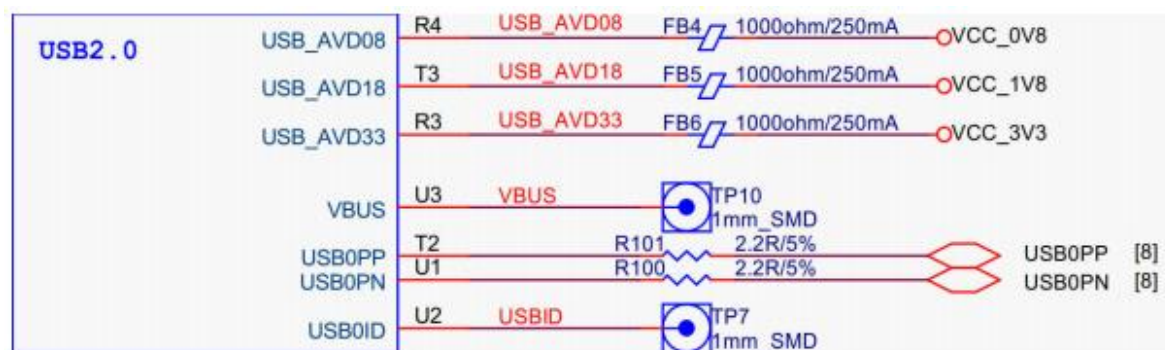
MIPI interface is used for DVP00 to DVP05 of DVP interface, and supports MIPI-CSI of 2lane. The multiplexing relationship is as follows:



USB OTG

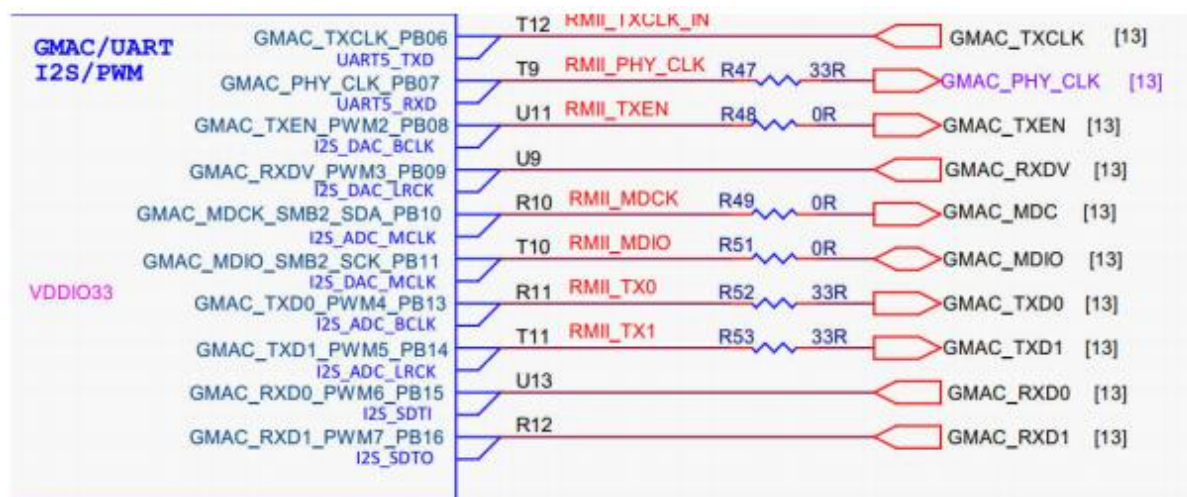
T41 USB interface supports OTG function. To configure it as OTG function, the USB_ID pin needs to be exported for use.

If it is simply used as the HOST or DEVICE function, the ID pin can be suspended, it can be solidified according to the software driver configuration of the product definition, and the VBUS pin can be suspended. If the product has high requirements for ESD level, it is recommended to connect 2.2 ohm resistor in series on the USB data line to strengthen the anti-static and surge capacity.



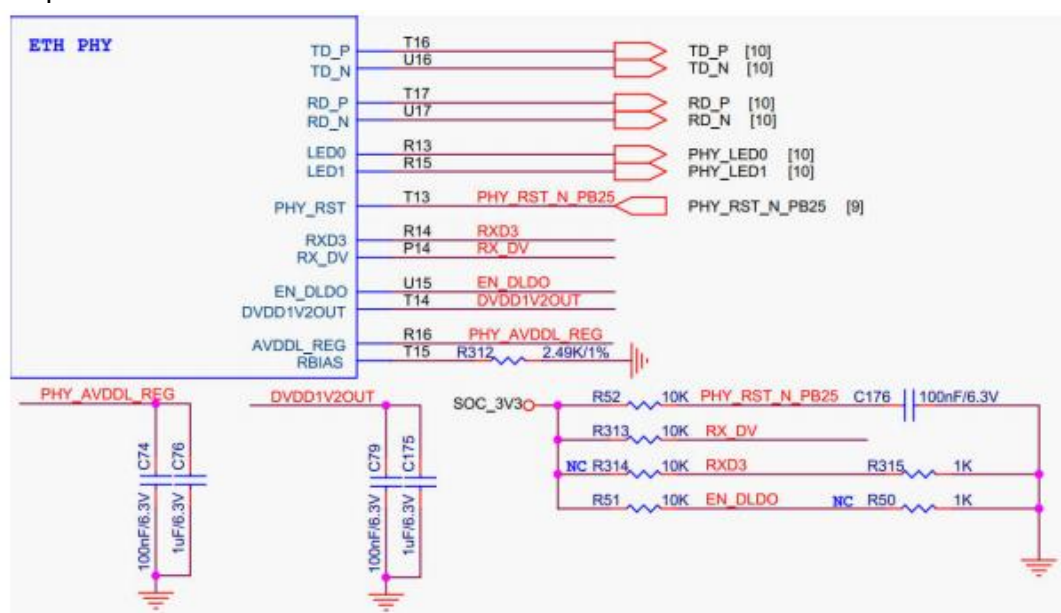
RMII network interface

T41 network interface supports RMII mode of 10/100M. The 25M/50Mhz clock required for external Ethernet PHY to work in RMII mode can be output through the pin of PB07 of T41; PB06 pin must be 50M input; MDIO needs to be connected with pull-up resistor; For MDCK, TXCK, TXD0, TXD1 and RXCK, RXD0, RXD1 signals, it is recommended to connect 33 Ohm resistors in series at the source end to obtain better signal quality.



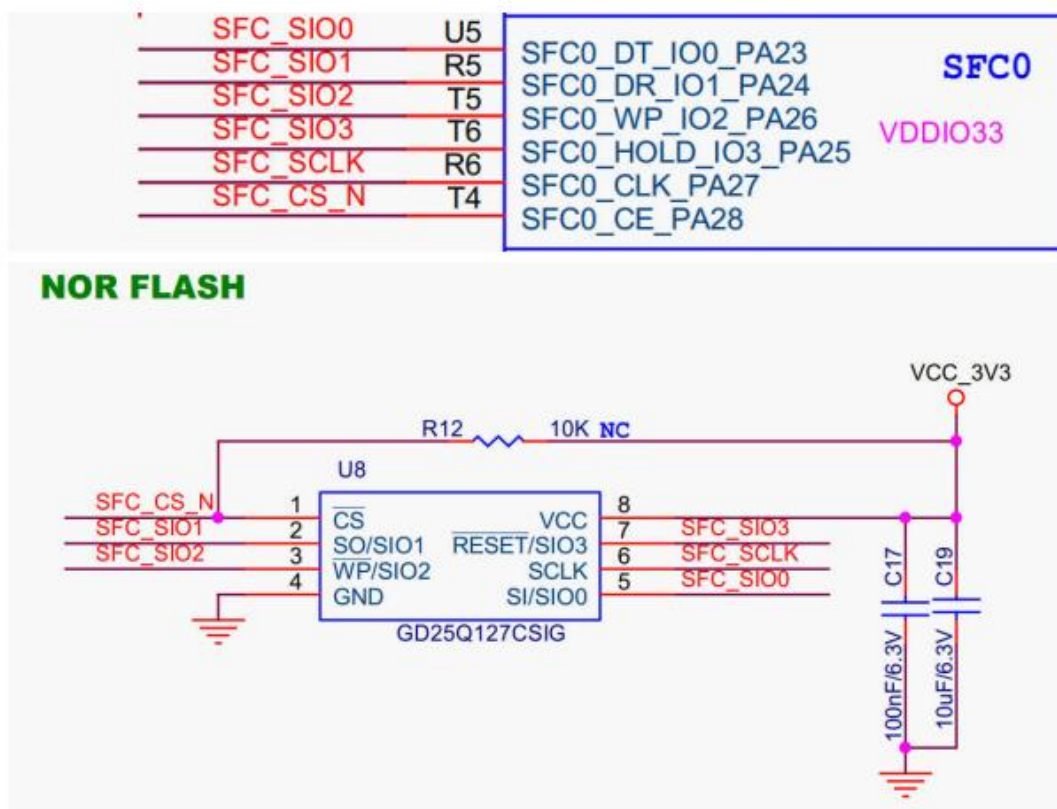
T41 also supports internal Ethernet PHY. The connection method is as follows: when using internal Ethernet PHY, RMII MAC interface cannot be used at the same time, and the corresponding pins need NC processing.

Note: internal Ethernet PHY and external Ethernet PHY share a group of MDIO interfaces, that is, when RMII network is used, GMAC_ MDCK (pin R10) and GMAC_ MDIO (pin T10) can only be used as MDIO interface, and GMAC_ MDIO (pin T10) needs to be pulled up to 3.3V and cannot be used for other functions.



SFC interface

T41 supports two-way SFC interfaces. SFC0 is distributed in PA23~PA28 of GPIO, and SFC1 is distributed in PA20~PA22&PA29~PA31 of GPIO. Both ways of SFC can be started as BOOT, and the interface can be connected to SPI NOR/NAND FLASH. The connection method is as follows:

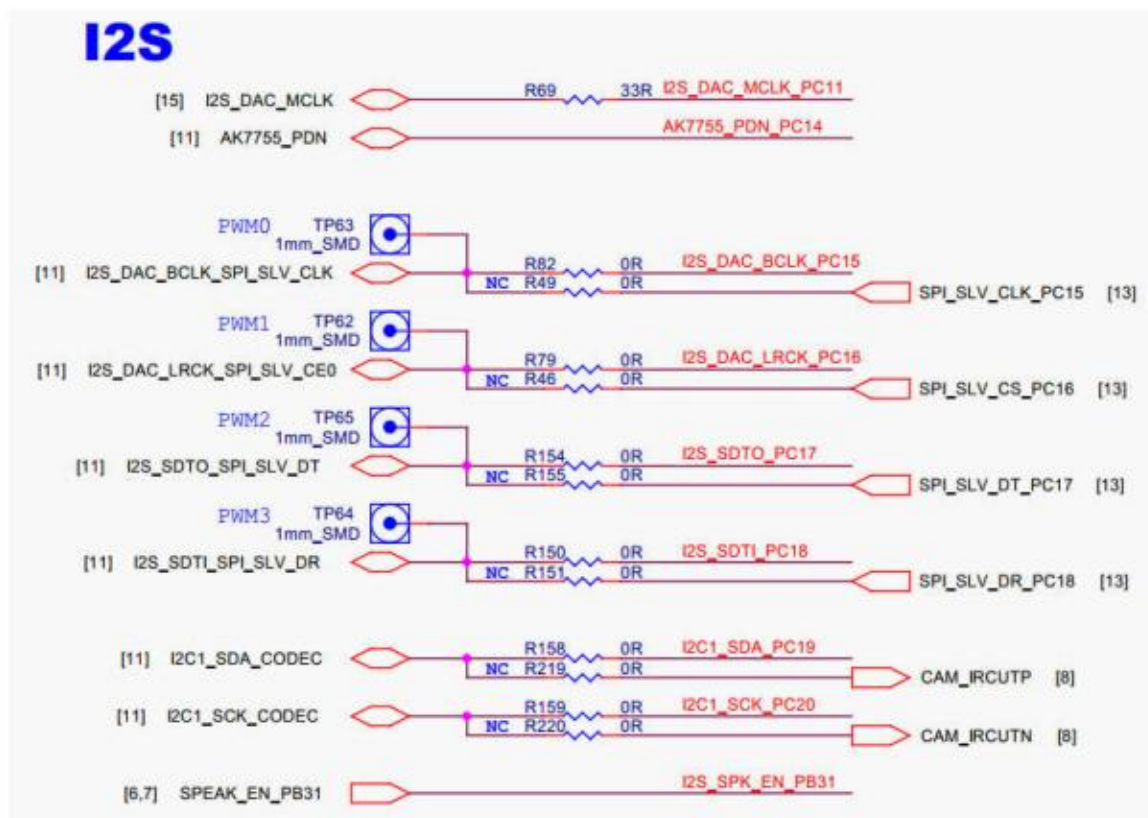


MSC interface

T41 supports two MSC interfaces. If an external TF card is connected, use MSC0 of PB00-PB05; If the SDIO WiFi module is connected externally, the MSC1 interface of PB17-PB22 can be used. Note that the MSC1 interface is also multiplexed in the PC group. On the low-power battery project, SDIO WiFi is connected to PC02-PC07, and the IO level is 1.8v/3.3V. For details, please refer to the <<T41 IPC product GPIO allocation recommendation table>>.

Audio interface

The built-in codec audio part of T41 supports one channel of analog input and one channel of analog output; Analog input supports differential and single ended modes; T41 supports one I2S bus, which is distributed in GPIO PB group or PC group. An audio codec can be connected externally through I2S. For general products, DAC clock is recommended for external audio codec. For details, please refer to the following:



SADC interface

T41 supports 4-channel 12 bit resolution ADC interface, and the reference voltage is ADC_ VREF, which can sample analog signals in the range of 0-1.8V. It is recommended to connect magnetic beads in series for ADC power supply. It is recommended to connect 2.2~10 Ohm resistors in series for channels used by ADC to enhance anti-static and surge capacity. Unused channels can be directly grounded.

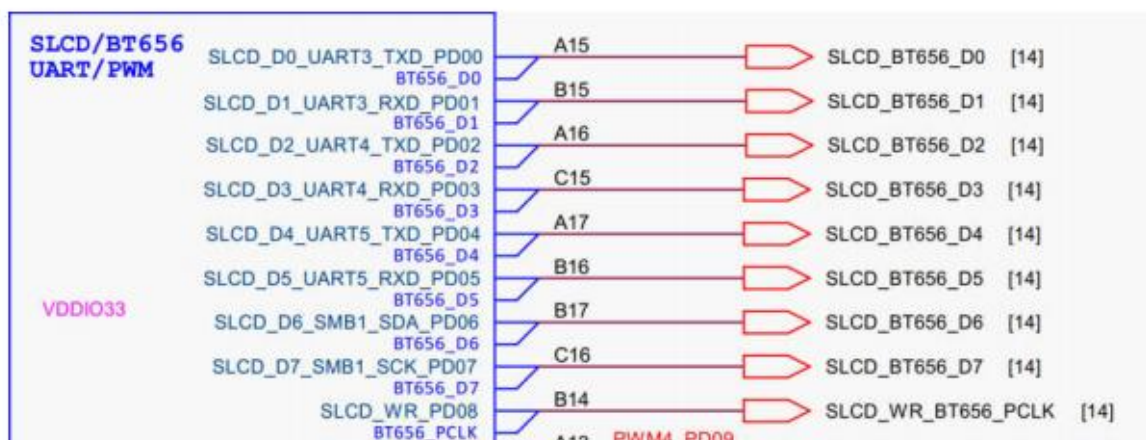
Efuse function

In burn mode, it is necessary to provide 1.8V+/-10% voltage to EFUSE_ AVD pin, and the burning time cannot exceed 1s; In read mode, The voltage of EFUSE_ AVD is 0V, which can be grounded through 0 Ohm resistance. EFuse in actual products_ AVD grounding is enough.

LCD interface

T41 supports the 8bit SLCD display interface, and the related function IO is distributed on the GPIO of PD group: the SLCD display interface multiplexes the BT656 output interface and BT1120 output interface at the same time (8bit serial mode). For the specific

GPIO multiplexing relationship, please refer to the <<T41 IPC product GPIO recommended allocation table>>.



Dmic interface

In addition to analog MIC input, T41 also supports up to 4-way dmic array input, as shown below.



2 PCB design considerations

PCB stack

T41 is a 0.65 pitch 232 pin BGA package, and the PCB stack design can adopt a 4-layer structure. **It is recommended that the adjacent layer of the main chip is the main GND layer, so that the main chip signal return path is the shortest.** If the main chip is laid out in the top layer, the stack is set to top-gnd-vcc-bottom. The top layer refers to L2, and the bottom layer refers to L3. The laminated structure is shown in the following figure:

layer		thickness
TOP	=====	1Oz
	PP	3(mil)
L2	=====	1Oz
	Core	Adjust according to plate thickness
L3	=====	1Oz
	PP	3(mil)
BOT	=====	1Oz

Layout considerations

- 1) Meet SMT process requirements.
- 2) High heat devices should be kept away from heat sensitive devices as far as possible. For example, CPU should be arranged away from CMOS sensors as far as possible.
- 3) Pay attention to the height limit position of the structure.

Vias setting

- 1) Ordinary vias adopts 8mil aperture and 16mil outer ring.
- 2) 12mil aperture and 24mil outer ring are used for ground and electric vias.
- 3) The vias arrangement of SOC main chip and DDR should be reasonable, and the spacing should not be less than 30mil, and the circuits of ground and electric layers should not be damaged.

Treatment of DDR power supply and ground

On the back of SOC main chip and DDR, it is best to place a decoupling capacitor corresponding to each power pin, and the vias should be placed next to the pin. The wiring should be as thick and short as possible to avoid increasing the inductance of the wire. The plane of VDDMEM and DDRVDD must ensure the actual routing width. When changing layers, try to drill as many through holes as possible to avoid becoming the bottleneck of the whole plane.

Crosstalk fundamentally depends on the stack of PCB and the minimum line spacing. The best way to avoid crosstalk is to ensure that the signal has a very good return path. Each signal layer should be close to the complete ground plane to provide the shortest return path. In order to keep the characteristic impedance consistent, it is very important that the ground plane is complete, and the ground plane cannot be interrupted. After the signal line is completed, the remaining space must be filled with GND, and the copper line width should be as small as possible, which can make the copper laying effect better.

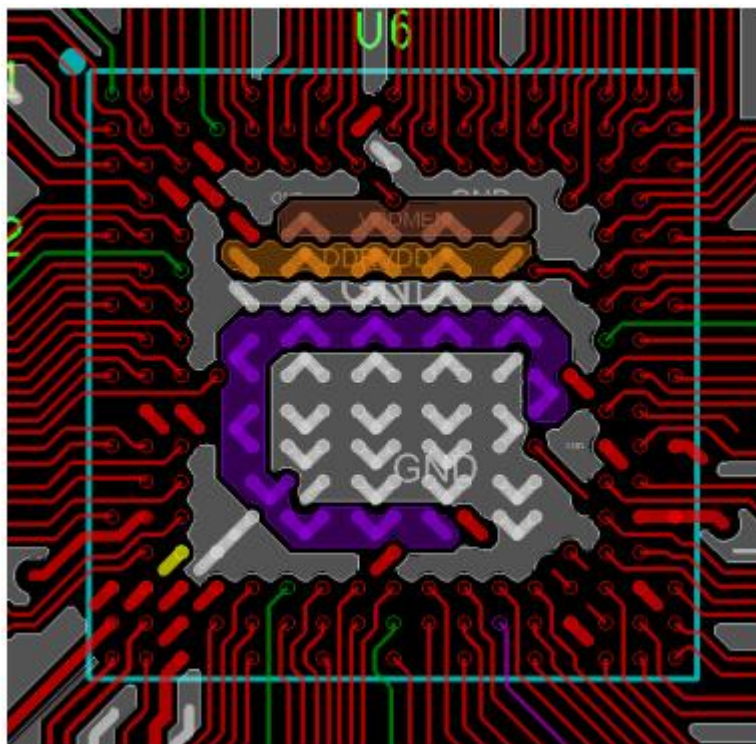
VREF is the reference of DDR input buffer. The VREF voltage dividing circuit should be as close to the chip as possible, and the wiring should be as short as possible. It is recommended to have a line width of 20 mil, and maintain a spacing of more than 3W with other data lines to ensure that it is not disturbed. Add a 0.01uF capacitor near the VREF pin.

Setting of copper laying

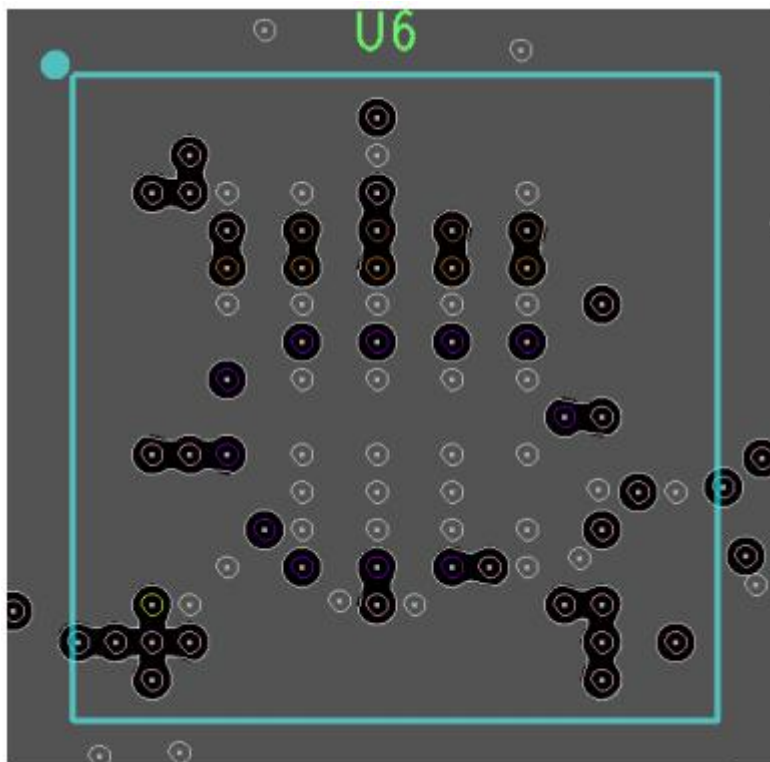
- 1) The safety distance between the vias and the copper laying is 6mil.
- 2) The laying copper wire width of the ground and electric layers is set to 2mil, and other layers can be set to 4mil.

Heat dissipation design

- 1) 1Oz is recommended for the thickness of copper and platinum to improve the heat dissipation performance of PCB.
- 2) After the SOC main chip is wired out, try to drill more ground holes without affecting the integrity of the power plane, as shown in the following figure:



3) The stratum must be complete, and there can be multiple paths inside the SOC main chip to connect with the outside of the SOC main chip.



4) The routing of high current should be as short as possible, and copper should be laid as far as possible to widen the routing width. At the same time, the thickness of this layer should be more than 1Oz. For the routing of the inner layer, it should be arranged in the adjacent layer of the formation.

5) The PCB board edge is surrounded by ground holes (through holes) and exposed copper, which is conducive to the metal grounding and ESD of the shell, as well as heat dissipation.

6) In the layout, the SOC main chip and other heating devices are separated by a certain width (at least 20mm), and the hottest devices are placed near them in a straight line by using the opening direction of the shell (such as cooling windows, large connector openings, etc.) (SOC main chip can be arranged in this way). For several heating devices, they shall be arranged in a cross manner and shall not be arranged in rows or columns.

Design of other power supplies

1) The power chip should be as close to the SOC main chip layout as possible.

2) During the layout of the power chip, we must pay attention to the position of the dc/dc input and output capacitors. The input and output capacitors should be as close to the dc/dc pin pin as possible, and ensure that the distance between their ground and the SOC main chip ground is as short as possible.

3) The filter capacitor of SOC main chip VDD, VDDMEM, DDRVDD, DDRPLL_VCCA, PLL_AVDD should be placed as close to the pin pin of SOC main chip as possible.

4) VDD, VDDMEM and DDRVDD need to lay copper on the power layer instead of wiring.

5) When changing the layer of the power supply, try to drill as many vias as possible to avoid becoming the transmission bottleneck of the power signal.

6) SOC main chip related capacitor layout:

Priority 1: DDRPLL_VCCA、PLL_AVDD、VDD、VDDMEM、DDRVDD、VREF.

Priority 2: USB_AVD33、USB_AVD18、USB_AVD08、CSI_VCC08、CSI_VCC18、VDD_RTC、CODEC_AVDD.

Priority 3: VDDIO18_1、VDDIO18_2、VDDIO2、VDDIO1_1、VDDIO1_2、VDDIO_RTC 、SADC_AVDD.

7) Ensure the integrity and continuity of the copper (ground and power) under the SOC main chip, so as to provide a good signal return path, improve the signal transmission quality and improve the stability of the product; At the same time, it can also improve the

performance of heat dissipation.

8) All grounding pads should be drilled through the nearest ground plane.

Crystal design

The signal routing of 24M crystal CLKIN and CLKOUT should be wrapping by the GND in the whole process, and the multilayer board design ensures that these signals have a complete reference. There should be no signal or power supply under the crystal circuit.

Clock routing

It is suggested that the whole clock routing should be wrapping by the GND, keep the 3W principle with other signals, and match the resistance in series to obtain better signal quality.

USB routing

In order to ensure good signal quality, the data signal line of USB2.0 port is wired in the way of differential line. In order to meet the speed requirements of USB 2.0 high-speed 480mhz, the following principles are recommended for PCB wiring design:

1) The routing of the differential data line shall be as short and straight as possible. The internal routing length of the differential data line shall be strictly equal, and the deviation of the routing length shall be controlled within $\pm 5\text{mil}$.

2) The differential data line controls a uniform differential impedance of $90\Omega \pm 10\%$.

3) The differential data line shall be routed on the wiring layer near the ground plane as far as possible without changing the layer.

4) The routing of the differential data line should have a complete ground plane as the reference plane, and cannot be divided across the plane.

5) The routing of the differential data line should use the least vias and corners as far as possible. The corners can be considered to use an arc or 135 degree angle to avoid right angles, so as to reduce reflection and impedance changes.

6) Avoid adjacent to other high-speed periodic signals and high current signals, and ensure that the spacing is greater than 50mil to reduce crosstalk. In addition, keep away from low-speed aperiodic signals and ensure a distance of at least 20mil.

DVP routing

The deviation between the length of data line and clock line shall be controlled within $\pm 300\text{mil}$; DVP_ MCLK、 DVP_ PCLK、 DVP_ HSYNC、 DVP_ Vsync wiring should maintain a distance from other wiring to meet 3W requirements to avoid crosstalk.

MIPI routing

Control the equal length within $\pm 5\text{mil}$ according to the difference line, control the difference between pairs based on the clock signal within $\pm 100\text{mil}$, and control the impedance within $100\ \Omega \pm 10\%$; Avoid the signal wiring passing through the power division area, and keep the signal reference plane intact; The distance between adjacent signal routes shall maintain the "3W" principle.

Audio routing

When wiring the audio part, the input and output wiring should be separated, and the MICP/MICN wiring should be differential, and the wrapping by the GND should be done to avoid the interference of other digital signals. The wiring of hpout shall be wrapping by the GND to avoid the interference of other digital signals and switching power supplies.

MAC routing

Due to the high rate of GMAC signal, it is recommended that PCB wiring design adopt the following principles to reduce the crosstalk between bus signals:

- 1) Avoid the signal routing passing through the power division area, and keep the signal reference plane intact.
- 2) The length of the signal line is based on the clock line, and the deviation of the routing length is controlled within $\pm 200\text{mil}$.
- 3) The ground directly below the transformer chip needs to be hollowed out.
- 4) The distance between adjacent signal routes shall maintain the "3W" principle.
- 5) It is recommended to connect a $33\ \Omega$ resistor in series with the clock signal to obtain better signal quality.

MDI_ TP、 MDI_ TN、 MDI_ RP、 MDI_ RN at PHY, the differential pairs should be as long as possible, the deviation of routing length should be controlled within $\pm 5\text{MIL}$, and the differential impedance should be controlled within $100\ \Omega \pm 10\%$.